Student Paper

High-field transport in monolayer graphene interconnects on chemical vapor deposited hexagonal boron nitride substrates

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The impressive electronic and thermal properties of graphene has made it one of the most important emerging research materials for on-chip interconnects. Graphene has been shown to possess high current breakdown density [1] and thermal conductivity [2], compatibility with IC fabrication [3], and resistance to electromigration [4], making the material a potential candidate for post-copper wiring. However, the dangling bonds and charge traps present in SiO_2 substrates greatly reduce the current carrying capacity and intrinsic properties of graphene [5]. Hexagonal boron nitride (hBN) dielectric substrates have been widely used to improve graphene performance due to its atomically smooth surface and small lattice mismatch (~1.7%). Thus far, high-field transport studies have been restricted to mechanically exfoliated hBN substrates, which do not offer scalability options for graphene-hBN device integration [6]. Here, we report on the fabrication and high-field characterization of vacuum-annealed monolayer graphene on stacked CVD hBN substrates, presenting a platform for graphene-hBN scaling.

Large-area monolayer hBN was synthesized by atmospheric pressure CVD on copper using an ammonia borane source, as confirmed by Raman spectroscopy (Fig. 1c). A 5-layer hBN stack is formed after consecutive transfers to an oxidized silicon substrate to provide sufficient isolation from the SiO_2. Monolayer CVD graphene ribbons of 3 μm in width were fabricated using standard electron beam lithography in the transfer length method (TLM) configuration on both 285 nm SiO_2 (Fig. 1a,b) and stacked hBN (Fig. 1c inset). Performance metrics were compared among as-fabricated devices in air, high vacuum (10^{-6} Torr) and current annealed samples on SiO_2 and hBN substrates in high vacuum. Current annealing was performed with a slow voltage ramp (~5 mV/s) to generate Joule heat, vaporizing resist residue carried over from the lithography process and improving contact resistance. Fig. 2a represents typical I-V characteristics for the high vacuum current annealing process, resulting in a decrease of device resistance from ~3.3 kΩ to ~1.3 kΩ and a decrease in contact resistivity from ~1.2 kΩ-μm to ~0.8 kΩ-μm (Fig. b and c). An improvement in sheet resistance and mobility, from ~400 cm^2/Vs to ~2000 cm^2/Vs, is also observed (Fig. c). Current annealed devices on hBN substrates showed slightly lower contact resistance (0.75 kΩ-μm) to devices on SiO_2 however a significant improvement in mobility (~9000 cm^2/Vs) and sheet resistance is seen (Fig. 2c).

To explore the performance and reliability limit of graphene interconnects, we electrically stressed the device until breakdown (Fig. 3a). Fig. 3b shows the breakdown characteristics of graphene ribbons from a channel length of 500 nm to 6 μm. We found that the greatest current density was achieved in short channels (Fig. 3c), likely due to reduced impurity scattering and lower device resistance while larger channel lengths sustained higher power (temperature) before breakdown (Fig. 3d), which suggests improved device cooling and better thermal dissipation due to a larger graphene-SiO_2/hBN contact area. Overall, graphene interconnects on CVD hBN substrates showed consistent improvements over SiO_2 (Fig. 3a-d). We observed over an order of magnitude improvement in mobility and sheet resistivity as compared with untreated devices on SiO_2 and achieved a room temperature current carrying capacity exceeding 9×10^8 A/cm^2 (>3 mA/μm). The resulting work provides a scalable method for improving transport properties via substrate engineering, benefiting applications where high-field performance and reliability are critical.

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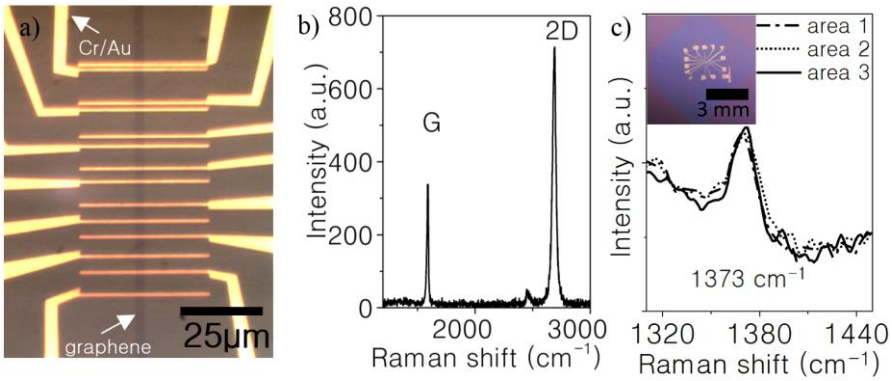

Figure 1. a) Optical micrograph of a 3 μm wide graphene ribbon contacted in the TLM configuration on 285 nm SiO_2. b) Raman spectra of post-fabricated device. c) Raman spectra of CVD hBN (three different areas) showing the characteristic peak centered near 1373 cm^{-1}. (inset) Large-area CVD hBN stack (5 layers) used as the substrate (appears dark purple) with TLM design pattered using ebeam lithography.

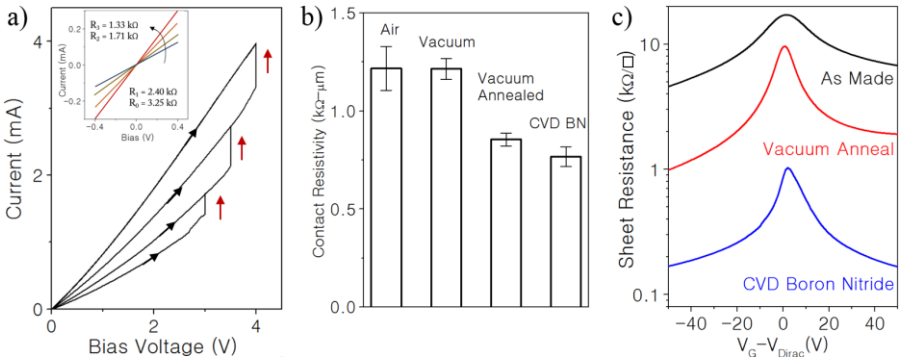

Figure 2: a) Current-voltage trace of consecutive high vacuum current annealing runs on the same graphene device. Bias is held at 3.0 V, 3.5 V, and 4.0 V for 10 min. b) Contact resistance extracted from TLM measurements showing a ~30% decrease after current annealing. c) Sheet resistance as a function of gate voltage for graphene devices before/after high vacuum current annealing and post-annealed on a pentalayer CVD hBN substrate.

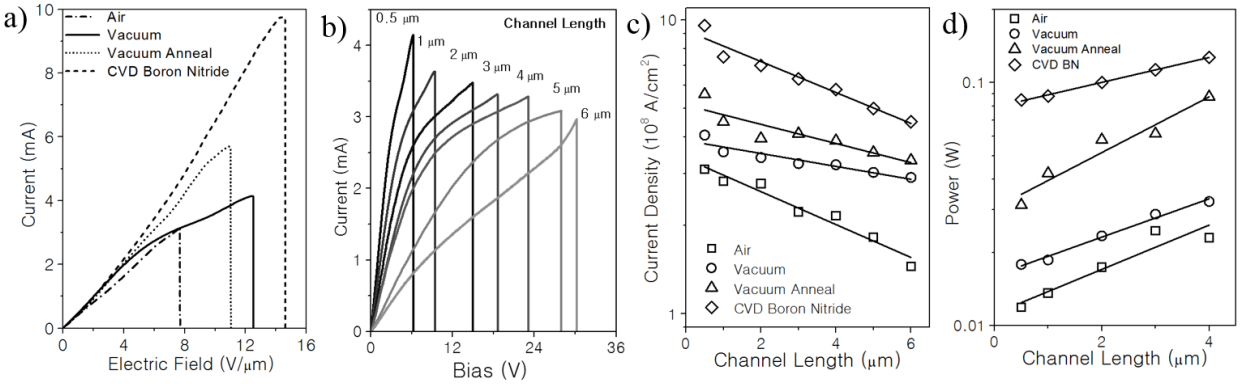

Figure 3: (a) Comparison of device breakdown at high-fields for 500 nm channel length devices. b) Breakdown characteristics of graphene ribbons of varying channel length. (c) Maximum current density of devices before breakdown. (d) Sustained power before device breakdown.