Quantum dot superlattice (QDSL) based multi-state MOSFETs and Junction Devices

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A QDSL layer is comprised of an array of individually cladded quantum dots (QDs) such as SiO_x (1 nm) -cladded Si (3-4nm) QDs and GeO_x-Ge QDs. QDSL is modeled as a superlattice which exhibits energy mini-bands. Each layer of cladded Ge/Si QDs represents a two-dimensional semiconductor. Unlike recently reported two-dimensional semiconductors [1], the energy band gap (as well as mini-band widths) can be tuned by the dot size, cladding thickness, and dot-cladding energy barrier heights [2]. We have demonstrated a variety of field-effect transistor structures incorporating QDSL layer either in gate or channel or both. In contrast to conventional FETs, they exhibit multi-state behavior that is relevant to multi-bit processing. These include: *(a)* 3-state ID-VG behavior in quantum dot gate (QDG) Si and InGaAs FETs (Fig. 3a)[2], where QDSL in the gate is separated from the channel by a very thin tunneling layer, *(b)* 4-state quantum dot channel (QDC) FETs (Fig. 3c)[3]; and *(c)* spatial wavefunction switched (SWS) FETs which comprise 2- or more quantum well/quantum dot channels exhibiting 4-state characteristics (Figs. 1, 2)[4]. This paper presents experimental I-V characteristics of p-Si/n-GeO_x-Ge QDSL devices showing steps, and explains carrier transport using superlattice mini-band model.

Figure 1a shows a 4-quatum well channel SWS-FET along with simulations of charge distribution at several voltages (Figs. 1b, 1c). Fig. 2a shows the C-V behavior of a fabricated InGaAs SWS MOS device (Fig. 1a), where the peaks show electrons in different quantum well channels. Fig.2b shows the experimental C-V for a quantum dot channel SWS MOS device showing multiple capacitance peaks in inversion as well as accumulation [4]. Figure 3a shows a Ge quantum dot gate (QDG) InGaAs FET with characteristics shown in Fig. 3b. QDC FET is shown in Fig. 3c with its measured multi-state Id-Vg characteristics in Fig. 3d.

Figure 4a shows the Ge QDSL mini energy bands computed using Kronig-Penny model [3]. Fig. 4b shows schematic cross-section of an n--Ge QDSL/p-Si diode. The diode characteristics are shown in Fig. 4c [5]. The injected holes recombine with electrons in the Ge-QDSL layer. Initially at low current values, the carrier transport is in the first mini-band which has a limited capacity to accommodate injected carriers. Once the mini-band is completely filled, the current saturates until an increase in the forward bias voltage reduces the separation between the Fermi level and the lower edge of the second mini-energy band. This is correlated with a step in I-V characteristics. From Fig. 4a, we can compute the magnitude of voltage at which the electrons from the second and 3rd mini-bands start to participate in current conduction.

Multi-state characteristics enable multi-bit logic and memory cells [6, 7]. These may result in significant space savings in microprocessors where SRAMs comprise significant die area.

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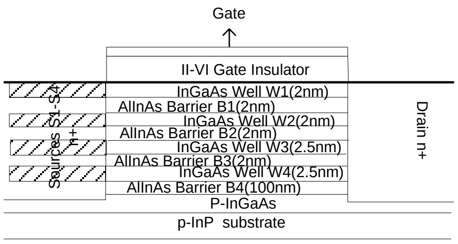

Fig. 1(a). 4 Well SWS-FET with InGaAs wells and AlInAs barriers.

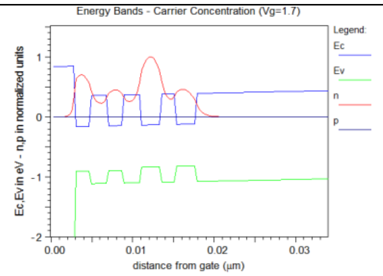

Fig. 1(b). Carriers mostly in well W3 (Vg=1.7V).

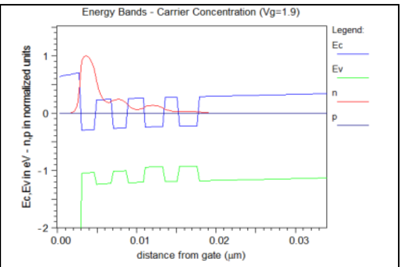

Fig. 1(c) Carriers mostly in well W1 (Vg=1.9V).

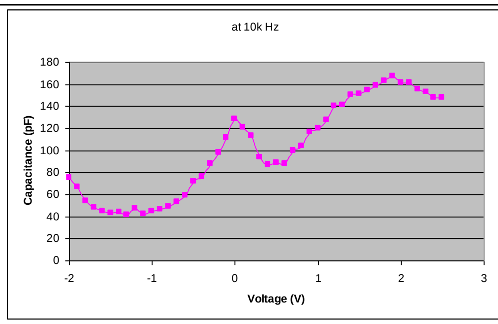

Fig. 2(a). C-V plot for a 4-well InGaAs SWS MOS device.

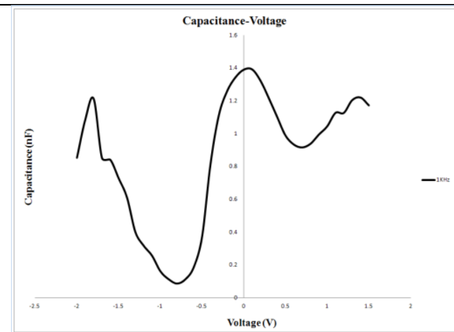

Fig. 2(b). C-V plot for a 4- layer SiOx-Si QD SWS MOS sample.

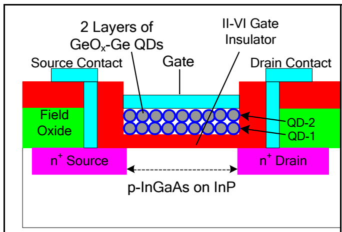

Fig. 3(a) GeO_x-Ge dot InGaAs QDG-FET.

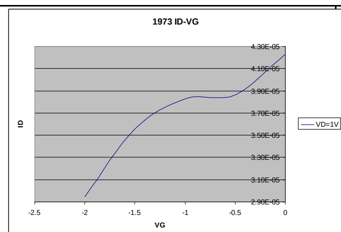

Fig. 3 (b) 3-state ID-VG of a GeO_x-Ge QD InGaAs FET (VD = 1V).

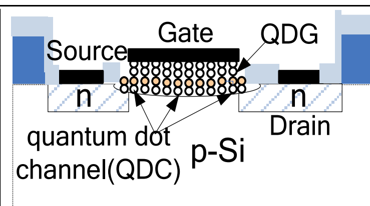

Fig.3(c). Schematic of QDC-FET

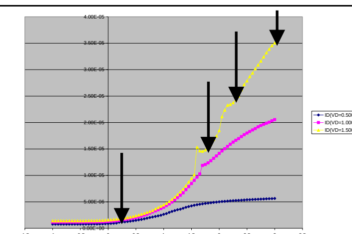

Fig. 3(d) Experimental Id-Vg showing multi-states.

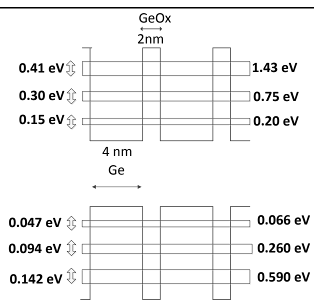

Fig. 4. GeO_x-Ge QDSL energy mini-bands.

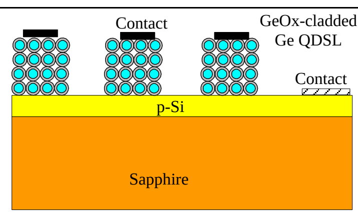

Fig. 5(a). GeO_x-Ge QDSL/pSi diode.

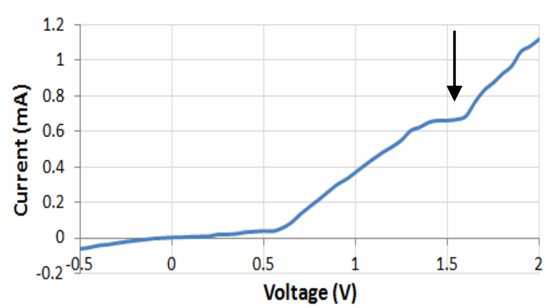

Fig. 5(b). I-V characteristic of the n--Ge QDSL/p-Si diode.