A New Non-Volatile Memory Architecture Embedding Microbatteries to Improve Data Retention Criterion

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As NVM technology gains maturity, new application fields emerge, often implying new product requirements, especially at high temperature. Thus, the data retention becomes a key criterion for good reliability cells. Many studies have already been performed on classical Flash or EEPROM memories to improve data retention of these devices [1,2]. Another approach consists in inventing and developing new non-volatile memory designs, with a higher robustness against charge leakage such as nanocrystal nonvolatile memories [3] or SONOS memories [4]. In this paper we describe a new cell design using floating gate architecture (Flash-type) and allowing to maintain the stored charge over long time. The proposed cell is based on a classical Flash design but the floating-gate (FG) is here divided in three parts as shown in Fig 1. The central FG will be used to store the charges injected during programming and erasing operations (Fowler-Nordheim mechanism) while the two lateral control gates (CG) will be used mainly in the retention phase. We can also remark that the tunnel oxide between the FG and the channel has not a constant thickness. Indeed it is thinner in the middle (around 7-8 nm) than at the sides (around 15nm). The thinner part will be used to inject charges in the floating gate while the thicker part will be used to retain charges during retention thanks to the addition of microbatteries in the circuitry which will allow to keep a positive bias on the two lateral gates, attracting electrons at the sides of the central FG over the thick oxide and thus reducing the charge leakage through tunnel oxide. Indeed, microbatteries have been improving rapidly for the last years and can now be integrated in microelectronics devices with small area and high capacity, using standard planar process [5] (with 50x50μm^2 for a 50nA.h capacity) or 3D micropatterned surfaces with nanowires [6]. This new structure has been simulated in a classical TCAD simulation tool (Synopsis Sentaurus Structure Editor) and is presented in Fig. 2. As described in Fig. 3 programming and erasing operations use the Fowler-Nordheim mechanism, which can even be enhanced thanks to the two lateral CG. The Synopsis Sentaurus Device electrical simulation tool is then used to apply the programming (duration=200µs) and erasing (duration=1ms) biases from Fig. 3, leading to a programming window (difference between the programmed and erased threshold voltages) of 3.2V, which is a viable value for a non-volatile memory, especially before optimization of the cell process (doping conditions, …). The threshold voltages of the virgin (no charge in the floating gate), programmed and erased cells (and thus the programming window) are plotted in Fig. 4. In the retention phase, Fig. 5 shows the battery positive bias (V_{+bat}) applied on the two lateral CG, attracting the electrons over the thick tunnel oxide. Nevertheless, we can notice that these electrons could leak through the thin lateral oxide between FG and lateral CG but this oxide is never damaged by charge injection (or only during the erasing phase in case of use of the lateral CG as presented in Fig. 3c)) and has consequently much less defects which can cause leakage. Moreover, if we consider that we lose all the stored electrons in a floating gate memory (typically less than 10^4 electrons after 10 years) [7], we can calculate the maximum number N_{max} of cells that we can bias with this battery, according to equation (1):

$$1A.h = 3600A.s = 3600C \Rightarrow 50nA.h = 1.8 \times 10^{-4}C \Rightarrow N_{max} = \frac{1.8 \times 10^{-4}C}{10^4 \times 1.6 \times 10^{-19}C} \sim 10^{11} cells \quad (1)$$

This shows that with only one elementary battery we can bias more than 10Gbytes for 10 years.

In conclusion, we have proposed an original Flash-type structure, integrating microbatteries in the circuitry to localize the stored charge over a thick oxide during the retention phase and thus supposed to improve the key reliability criterion. We have developed a full TCAD simulation of our structure showing the feasibility of this cell with a 3.2V programming window before process optimization and more than ten years of battery life for more than 10Gbytes.

References

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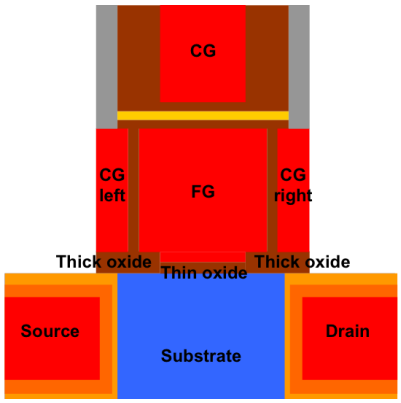

Fig. 1: Schematic view of the proposed structure.

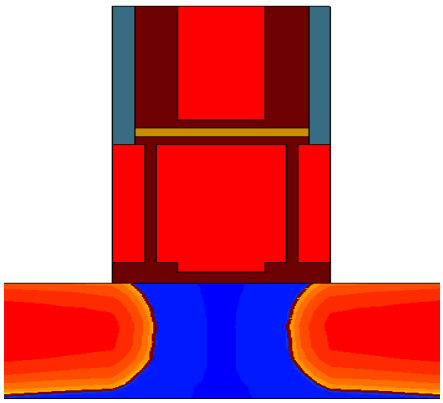

Fig. 2: TCAD simulated structure in Structure Editor Sentaurus tool.

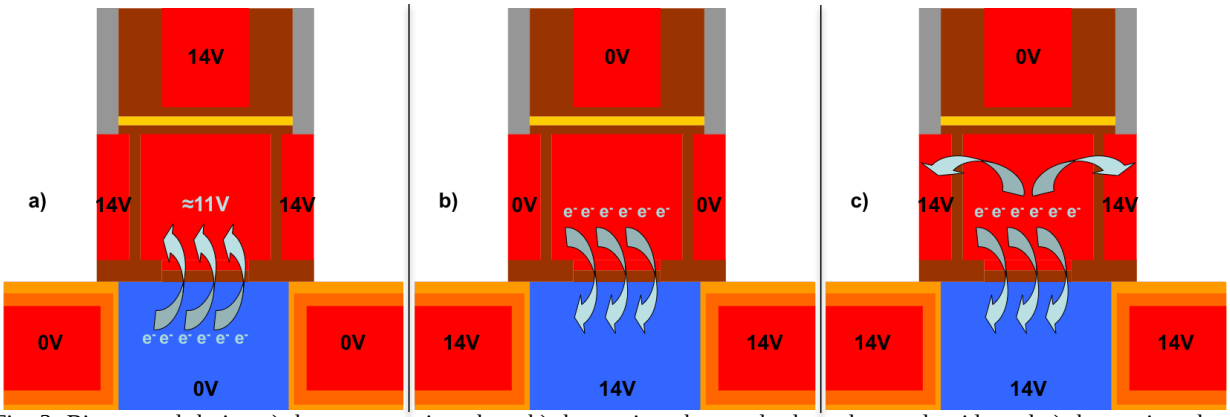

Fig. 3: Biases used during a) the programming phase b) the erasing phase only through tunnel oxide and c) the erasing phase using also lateral oxides to improve the erase efficiency.

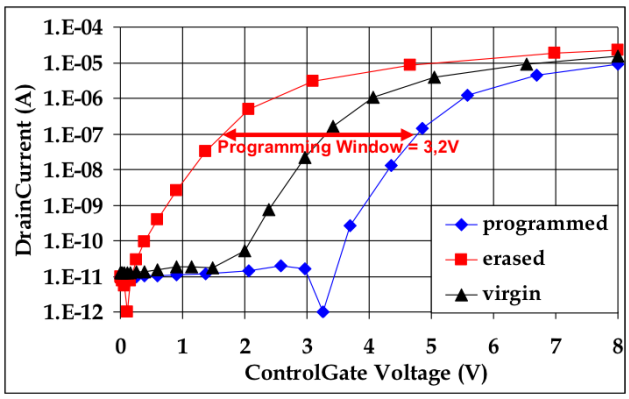

Fig. 4: Simulation of the programming window.

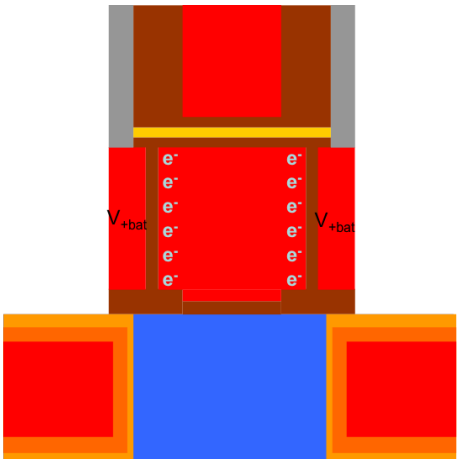

Fig. 5: Battery positive bias applied on the two lateral CG.