Sensitivity analysis of Super-Lattice FETs to technological and design parameters

P. Maiorano, E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani
ARCES and DEI, University of Bologna, Italy, pmaiorano@arces.unibo.it.

Abstract. We carry out an investigation on the sensitivity of the electrostatically-doped SL-FET to technological and design parameters. Electrostatic doping ensures a relatively low sensitivity to (i) channel length, (ii) SL barrier and well thicknesses, (iii) source/drain doping concentrations, and (iv) misalignments of the gate and SL electrodes. Moreover, at V_{DD} = 0.4V the proposed device is predicted to have 1.6× lower static power consumption than ITRS HP projections for year 2022.

Introduction. Low supply-voltage operation is mandatory to support new functional improvements which are needed to develop thinner, lighter and more sophisticated products with an acceptable battery life. One of the most promising device concepts is based on the idea of lowering the inverse subthreshold slope SS by filtering out high-energy electrons via a superlattice (SL) heterostructure in the source extension. Previous analyses [1,2] showed exciting results, outperforming the ITRS specs. Key element of this device is the SL structure which requires multiple barrier (*b*) and well (*w*) layers. In order to obtain optimum performance, the well regions must be doped to keep the SL potential as uniform as possible [2]. However, uniformly doping very thin semiconductor layers is a serious technology challenge. In this work we explore feasibility of an electrostatically doped SL [3] and investigate its scaling properties and sensitivity to technological and design parameters.

Design structure. Fig. 1 sketches the cylindrical nanowire geometry of the investigated device with impurity doping (ID) and electrostatic doping (ED), i.e. by inducing the required amount of charge carriers by an appropriately biased gate contact surrounding the SL region. The investigated SL-FETs are realized with InGaAs/InAlAs and InGaAs/InP material pairs [2]. A quantum-mechanical treatment able to take into account non parabolicity effects is carried out, and ballistic transport is assumed.

Effects of the SL electrostatic doping. Turn-on characteristics of the SL-FETs with D = 10 nm at V_{DS} = 0.4V with both ID and ED in the SL are shown in fig. 2. The two doping approaches are compared to target LSTP specs on I_{OFF}. To this aim, a similar energy barrier must be ensured at the SL/Ch junction of the two device types. As shown in fig. 3, the SL gate of ED devices screens the SL potential from the influence of the gate bias, thus inducing a barrier lowering at the SL/Ch junction compared to an ID case with similar degeneracy. Thus, lower degeneracy is needed in the ED case to provide an equal I_{OFF}, which is obtained by properly choosing the bias V_{SL} and position of the SL gate. This degrades I_{ON} compared to that of ID devices [fig. 2 left], while the SS remains well below 60 mV/dec in all SL-FETs [fig. 2 right]. However, the I_{ON} level of about 1mA/um achieved with ED is nearly flat as the I_{ON}/I_{OFF} ratio changes by several orders of magnitude. In turn, SS is below 40mV/dec for 6 decades [fig. 4 bottom].

Sensitivity to technological and design parameters. Sensitivity of the electrostatically-doped SL-FET to technological and design parameters has been carefully investigated considering (i) gate length L_G, (ii) SL *b* and *w* thicknesses, (iii) source/drain doping concentrations, and (iv) misalignments of the gate and SL electrodes. The InGaAs/InAlAs results are illustrated here, but similar conclusions apply to InGaAs/InP. Fig. 5 shows that SS < 30 mV/dec whenever L_G > 30 nm. We have also verified that decreasing the number of barriers down to 7 does not affect I_{ON}, although it causes a small SS degradation (not shown). More critical is the variation of the SL periodicity (fig. 6). Increasing *b* by two atomic layers with respect to the optimized *b* values degrades I_{ON} by about one order of magnitude. The worst case is the simultaneous increase of *w* and *b* layers. Device sensitivity to source (N_S) and drain doping (N_D) is shown in fig. 7. Reducing both N_S and N_D increases the off-state leakage and switching voltage, while I_{ON} is only marginally affected. Misalignments of the gate and of the SL electrode are treated in figs. 8 and 9, respectively, and turn out to marginally affect device performance. Finally, table 1 provides a performance comparison between ITRS specs and the two ED SL-FETs.

Conclusions. We have investigated the sensitivity of electrostatically-doped SL-FETs to technological and design parameters. Electrostatic doping guarantees a low sensitivity and is able to screen the gate impact on the SL energy potential profile. Finally, at V_{DD} = 0.4V the proposed device is predicted to have 1.6 × lower static-power consumption than ITRS HP projections to year 2022.

References

[1] E. Gnani et al., "Steep-slope nanowire FET with a superlattice in the source extension", *Solid-State Electronics*, vol. 65, pp. 108-113, 2011.
[2] E. Gnani et al., "Performance limits of superlattice-based steep-slope nanowire FETs", *IEDM*, pp. 5.1.1- 5.1.4, 2011.
[3] J. Appenzeller et al., "Toward Nanowire Electronics", *IEEE Transactions on Electron Devices*, vol. 55, pp. 2827-2845, 2008.

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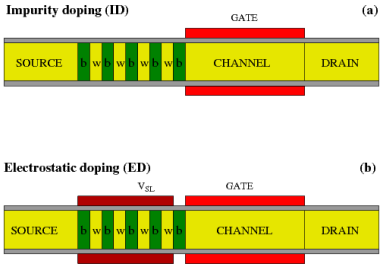

Fig 1: Pictorial view of the SL nanowire cross section. The SL is made by multiple barrier and well layers, and is interposed between the source and the channel. In principle, the SL region can be doped either by impurities (a) or electrostatically (b) by a gate electrode surrounding the SL region [3]. The gate dielectric is assumed to be Al_2O_3 with an equivalent thickness EOT = 1 nm. Finally, D = 10 nm and L_G = 60 nm.

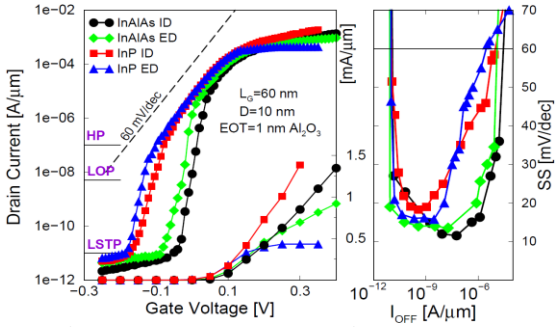

Fig 2: Left: Drain current at V_{DS} = 0.4V for the SL-FETs based on InGaAs/InAlAs and InGaAs/InP, with both ID and ED. Bias (V_{SL}) and position of the SL gate were adjusted to obtain LSTP-compatible off-state current I_{OFF}, thus requiring the electrode to be aligned with the last well (see fig. 1) and V_{SL} = 0.2 V. Such value causes I_{ON} degradation with respect to the ID case for the reason explained in fig. 3. I_{OFF} limits for LSTP, LOP and HP applications are indicated. Right: Point SS as a function of I_D, along with the 60 mV/dec SS limit. SS remains well below 60 mV/dec for over 4 current decades.

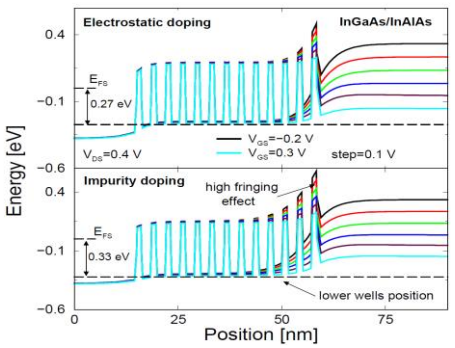

Fig 3: Subband energy profiles along the channel at different gate voltages in the ED (top) and ID (bottom) SL region of the transistor. The SL gate screens the potential from the influence of the Ch-gate, and lowers the barriers at the channel end of the SL, thus raising I_{OFF}. In order to fulfill the ITRS LSTP spec, the V_{SL} bias is tuned to reduce carrier degeneracy within the SL, thus lowering the on-state current I_{ON}.

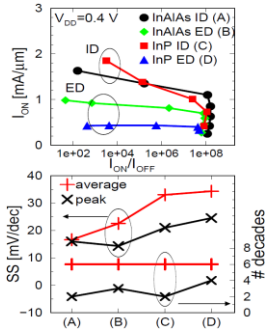

Fig 4: I_{ON} as a function of the I_{ON}/I_{OFF} ratio (top) and peak/average SS (bottom) and number of decades over which SS is stable. I_{ON} is nearly flat across several orders of magnitudes of the I_{ON}/I_{OFF} ratio and SS is lower than 40 mV/dec for 6 decades.

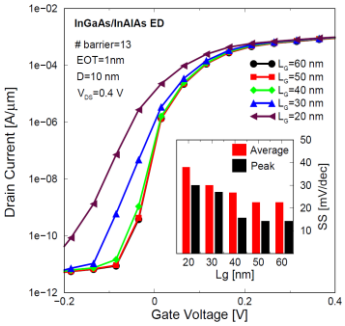

Fig 5: Turn-on characteristics of the InGaAs/InAlAs ED-doped SL-FET. As the gate length varies from 20 to 60 nm, the device characteristics in subthreshold are scarcely affected by SCE. Inset: Subthreshold slope SS for the same device.

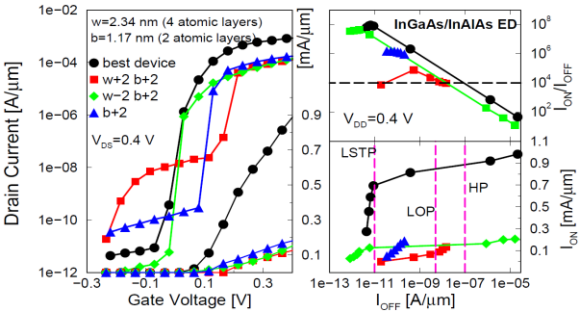

Fig. 6: Turn-on characteristics vs. number of atomic layers within the SL barriers and wells (2 and 4 respectively for the optimized device). *b* is a crucial design parameter: its increase by 2 atomic layers with respect to the optimal value decreases I_{ON} by about one order of magnitude. The worst case occurs for a simultaneous increase of *w* and *b* layers. The reason for the huge current changes is because changing the length of *b* and *w* shifts the filter band-pass and provides different miniband extensions and positions with respect to the Fermi level. Right: I_{ON}/I_{OFF} ratio (top) and I_{ON} (bottom) against I_{OFF}. The increase of *b* and *w* is detrimental for both I_{ON}/I_{OFF} ratio and on-state performance.

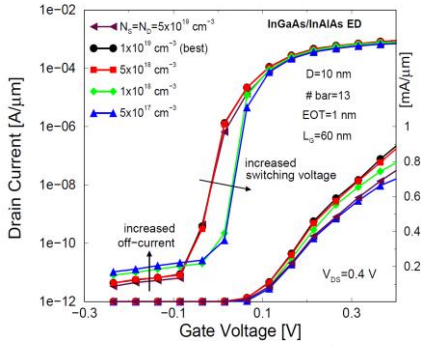

Fig 7: Turn-on characteristics of the InGaAs/InAlAs ED device at V_{DS} = 0.4 V for different N_S and N_D. Reducing both N_S and N_D, an increase of the off-state current and switching voltage occurs, while the on-state current is only marginally affected. This effect is again due to changes in the energy minibands.

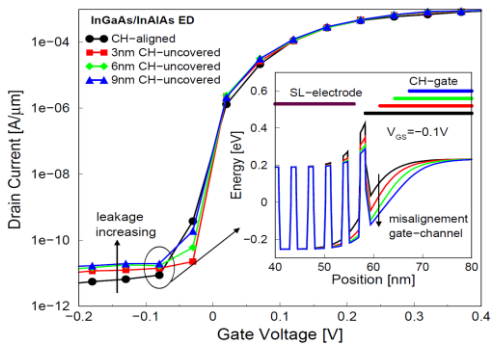

Fig 8: Transfer characteristics of the InGaAs/InAlAs ED device against misalignment of the gate contact with respect to the channel, as depicted in the inset. Widening the gate-channel underlap causes I_{OFF} to increase due to the weakened electrostatic coupling between the gate and the SL potential energy. This coupling provides a higher energy barrier (see inset), hence a lower current.

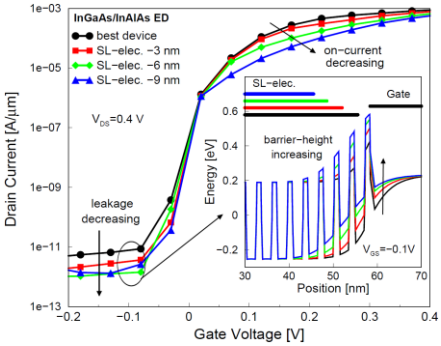

Fig. 9: Transfer characteristics of the InGaAs/InAlAs ED device against misalignment of the SL electrode as depicted in the inset. The misalignment increase results in a lower I_{OFF} due to the weakened electrostatic control of the SL electrode and the increased barrier height at the SL-Ch junction (see inset). However, higher barriers are detrimental for I_{ON}.

	HP	InAlAs	InP	LOP	InAlAs	InP	LSTP	InAlAs	InP
I_{ON} [mA/μm]	2.03	0.89	0.465	0.759	0.81	0.44	0.538	0.61	0.34
V_{DD} [V]	0.64	0.4	0.4	0.49	0.4	0.4	0.63	0.4	0.4
EOT [nm]	0.56	1	1	0.63	1	1	0.75	1	1
Static power [nW/ μm]	64	40	40	2.45	2	2	$6x10^{-3}$	$4x10^{-3}$	$4x10^{-3}$
Static power saving $P_{leak}^{ITRS}/P_{leak}^{SL}$	–	1.6	1.6	–	1.2	1.2	–	1.5	1.5

Table 1: Comparison of the ITRS goals (year 2022) with the data of the SL devices. We fix I_{OFF} at the ITRS values, and report the data extracted at V_{DD} = 0.4 V (roughly half of the ITRS values), and with EOT = 1 nm (rather conservative). The InGaAs/InAlAs device improves upon the ITRS I_{ON} specs for the LOP and LSTP applications, but lags behind the HP spec. Instead, the SL static energy dissipation outperforms the ITRS requirements for all applications.