A Fully Two-Dimensional Simulator of Quantum Well (QW) III-V FETs: Short Channel and Gate Tunneling Effects.

A.Gili, J.P.Xanthakis and A.Anastasopoulos

Electrical and Computer Engineering Department, National Technical University of Athens, Zografou Campus, Athens 15700, Greece, jxanthak@central.ntua.g.

MOSFETs with III-V compound semiconductor channels called III-V MOSFETs or Quantum Well (QW) FETs are a possible replacement of Si/SiO_2 transistors. Both Al_2O_3 and HfO_2 have been tried as gate oxides while InGaAs is the most usually chosen channel material in conventional and buried form channels [1-3]. At the moment these transistors are fabricated with large gate lengths Lg [4] but to produce superior performance to the Si/SiO_2 MOSFET they must have an Lg in the nanometer range. At such gate lengths quantization effects in both the vertical (gate to substrate) and horizontal direction (source to drain) are important. Hence a fully two-dimensional simulation method- i.e. one in which all Poisson, Schroedinger and Continuity equations are solved in two dimensions- is necessary to predict behavior at small gate lengths.

Here we produce such a simulation tool and we test it against the experimental data of the QW FET described in [4] which consists of the following set of consecutive layers: $Al_2O_3/In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$. This simulation follows our previous work on HEMTs [5] and on buried channel QW FETs [6]. We emphasize that all parameters of our model have been obtained from independent sources, i.e. no fitting has been used except for the Schottky barrier Φb at the metal oxide interface for which there is no information. In particular, the band edge offsets between the Al_2O_3 oxide and the semiconductor layers have been obtained from Robertson and Falabretti [7] while the drift diffusion mobility models from Palankovski and Quay [8]. The charge density n(x,y) below the source and drain regions and in the substrate is obtained by the use of the Fermi integral. Below the oxide a quantum box is constructed which includes the supply and channel layers and in which the Schroedinger equation is solved in two dimensions in order to obtain the quantized n(x,y). For transport across different semiconductor layers the theory of Lundstrom [9] is used in the drift-diffusion equations.

Our calculated charge density over the whole of the device is shown in figure 1. Note the formation of the channel below the over-doped source (S) and drain (D) regions which is shrinking near the D end. The variation of the current as the gate voltage Vg is varied is shown in figure 2 together with the experimental curve. Note that the scale is logarithmic, so this figure includes the subthreshold region also. Given that we have not fitted any parameters it looks as if we have a good agreement with the experiment. Having validated our model we proceed to examine its behavior at small Lg. The change in threshold voltage V_T is shown in figure 4 (as deduced from figure 3) and it appears linear. It is estimated to be 0.2V per 100nm change in Lg. The increase in current - standardized at Vd=Vg=2V- as Lg decreases is shown in figure 5. A value of 500mA/mm is predicted at Lg=35nm. Finally figures 6 give the band diagram along a vertical cut at the middle of the device at Vg=0V and Vg=2.5V.From this figure we deduce that at small Vg tunneling occurs from InGaAs to the metal electrode and at higher Vg the opposite is true. We also note that the barrier remains trapezoidal at all Vg ensuring very small tunneling while the field inside the oxide is approximately 0.04V/nm, further ensuring small gate tunnel current. A WKB calculation of the transmission coefficient gives an Id at Vg = 2.5V much lower than pA/mm.

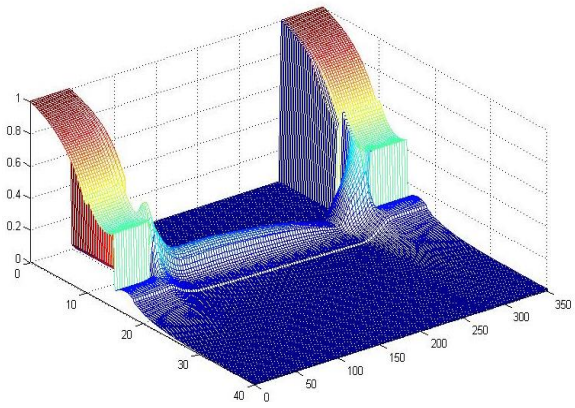

Figure 1: 2-D calculated charge density for the device of ref.4

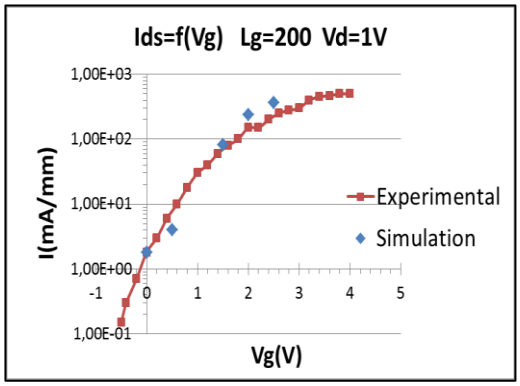

Figure 2: Variation of current with gate voltage Vg (solid line) contrasted to experimental values.

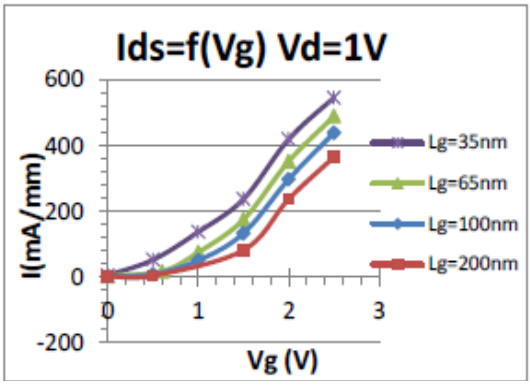

Figure 3: The variation of the current Ids as a function of Vg for different gate lengths.

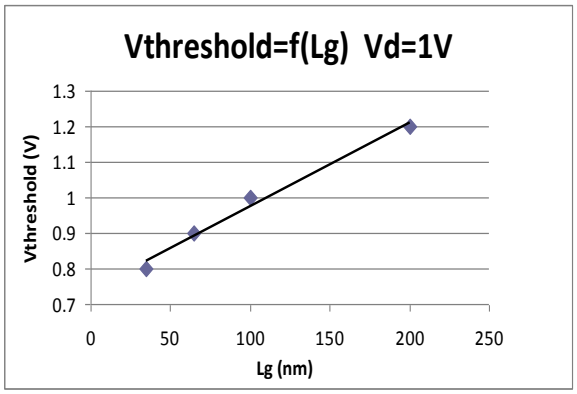

Figure 4: Change in threshold voltage V_T as Lg increases.

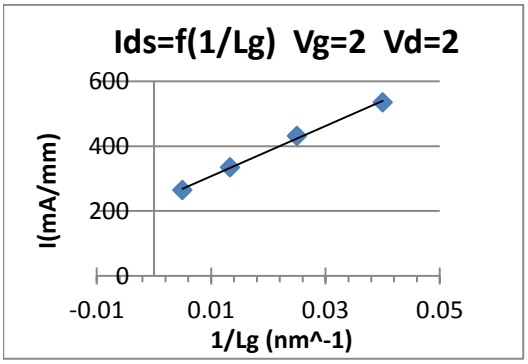

Figure 5: Variation of the current -standardized at Vd=Vg=2V–as the gate length Lg decreases.

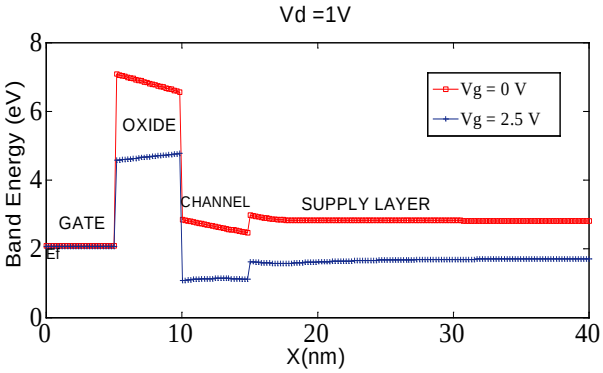

Figure 6: Band diagram along the depth of the device at its medium

References

1.S. Oktyabrsky, V.Tokranov et al, Journal of Crystal Growth, 311, 1950–1953, (2009).
2.Han-Chung Lin, Wei-E. Wang, et al, Microelectronic Engineering, 86, 1554–1557, (2009).
3.M. Yokoyama, R. Iida et al IEDM 2010.
4.Uttam Singisetti, Mark A. Wistey, et al, IEEE Electron Device Letters, 30, 1128-1130, 2009.
5.G. Krokidis , J.P. Xanthakis , N.K. Uzunoglu, Solid-State Electronics 52, 625–631, (2008).
6.I.Tsopelas A.Gili, J.P.Xanthakis, Key Engineering Materials, 495, 112-115 (2012).
7.J.Robertson and B. Falabretti, J. App. Phys., 100, 014111 (2006).
8.V.Palankovski and R.Quay, Analysis and Simulation of Heterostructure Devices, Springer, Wien/New York, 2004.
9.R.J. Schuelke and M.S.Lundstrom, Solid State Electronics, 27, 1111, 1984.