Negative Bias Temperature Instability in devices with millisecond anneal induced for ultra-shallow junctions

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Introduction. Ultra shallow junction formation in deeply scaled CMOS technologies requires the optimization and control of the implanted dopants. To achieve this objective millisecond anneal (MSA) has been shown to be a promising technique for the 32nm node and below [1]. On the other hand, Negative Bias Temperature Instability (NBTI), one of the main aging mechanisms in CMOS devices, is strongly dependent of the fabrication process [2]. Although some prior work has been done about the influence of MSA on NBTI degradation [3], here we will extend these studies from very short to medium relaxation times. Moreover, the results will be interpreted in the framework of the recent advances in the NBTI physics modeling.

Experimental. The samples used in this work were pMOS transistors with $HfSiO/Al_2O_3$ with TaCN as gate electrode and W/L=10μm/0.15μm. The MSA was applied for the activation of the source/drain implantations by means of a laser pulse on transistors; low (LLP), medium (MLP) and high (HLP) laser powers were studied. The temperatures achieved during the three types of annealing are estimated to be 1100ºC, 1200ºC and 1350ºC; the duration of each anneal is around 1 ms. To provoke the NBTI degradation, constant voltage stresses (CVS) of 10s, 100s and 200s were applied. After each CVS the devices were relaxed during 150s. The threshold voltage was measured during the relaxation using an ultra-fast (UF) set up [4] (fig. 1). The system operates at two modes, measure or stress, which can be interchanged by means of three digital switches. At the stress mode, a CVS is applied to the device; at the measure mode, 100mV were applied to the drain and the source was grounded. In this mode a current through the channel is forced by means of I_{bias}. If the value of I_{bias} is properly chosen, the transistor operates at $V_G=V_{th}$. Finally V_{th} evolution during relaxation is measured using an oscilloscope. With this setup values of V_T can be obtained after 20us of relaxation. Note that the negative feedback of the amplifier is maintained when the modes are interchanged, avoiding voltage ripples that could be detrimental for the measurement.

Results. Figure 2 shows the fresh (non-stressed) Id-Vg characteristics in linear and semilog scale. Clearly, a high V_{th} shift reduction is observed for MLP and HLP conditions [1]. In figure 3 the BTI relaxation traces after the CVSs are plotted. Increasing the laser power significantly reduces the NBTI degradation, which could be related to a annihilation of defects at high temperatures during the MSA. To model the V_{th} traces in figure 3, the occupancy maps (that is, the probability that a defect with given emission and capture times is occupied) at the measurement conditions have been calculated [4,5]. The defects were considered to follow a bivariate distribution in the $\log(\tau_e)$-$\log(\tau_c)$ map (a second bivariate distribution should be considered for long stress and relaxation times or extrapolations) [6]. Figure 4 shows the distribution obtained for samples with LLP, MLP and HLP. Note that similar distributions are obtained for the three types of samples; however the k parameter, which is proportional to the number of active defects, decreases with the laser power. Finally, the V_{th} shift obtained at different stress voltages can be fitted by an exponential law (figure 5). A very similar exponent (α) is obtained for devices with different laser power anneal, which supports the hypothesis of defect passivation by the annealing.

Conclusions. NBTI degradation in pMOS transistors with high-k dielectric has been studied when a millisecond anneal is used for ultra-shallow junction implantation using different laser powers. The results show that V_{th} degradation caused by NBTI can be correctly described using the occupancy maps of defects within the device, moreover the defect distribution in the emission-capture times space can be obtained. The laser power significantly reduces the BTI degradation, improving the device reliability. This effect has been associated to the defect passivation during the device annealing.

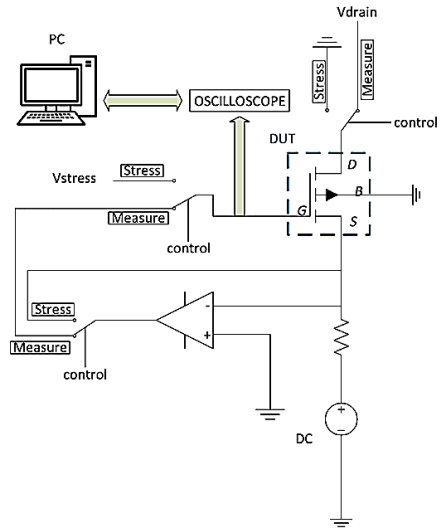

Fig. 1. Schematic setup used to perform Ultrafast measurements.

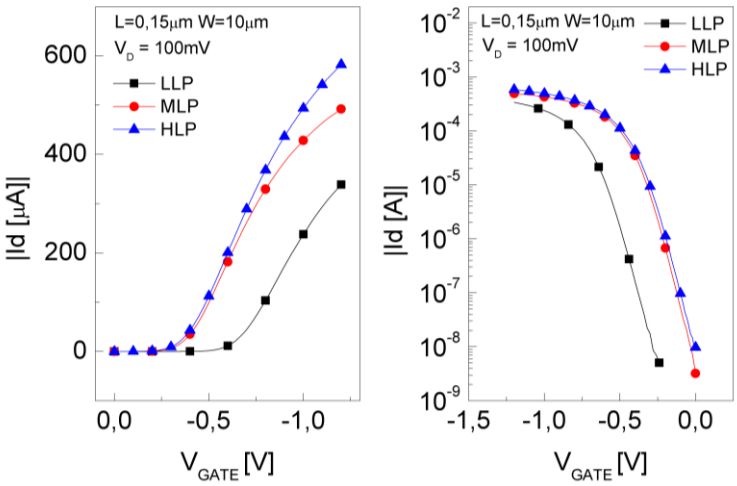

Fig. 2. Id-Vg characteristic in linear (left) and semilog (right) scale of fresh devices. Transistors with LLP show a higher threshold voltage.

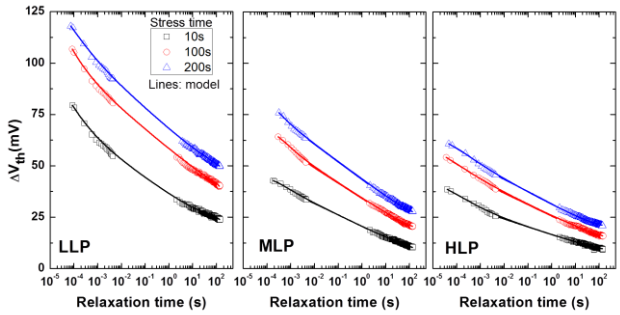

Fig. 3. V_{th} shift as a function of relaxation time obtained after stresses at -2.1V. Increasing the power of the laser anneal significantly reduce the NBTI degradation.

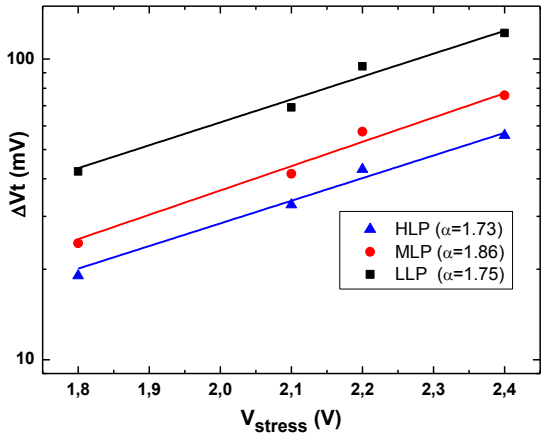

Fig. 5. V_{th} shift as a function of stress voltage for different powers of the laser anneal. The V_{th} shift values where obtained after 10s of stress and 0.3s of relaxation.

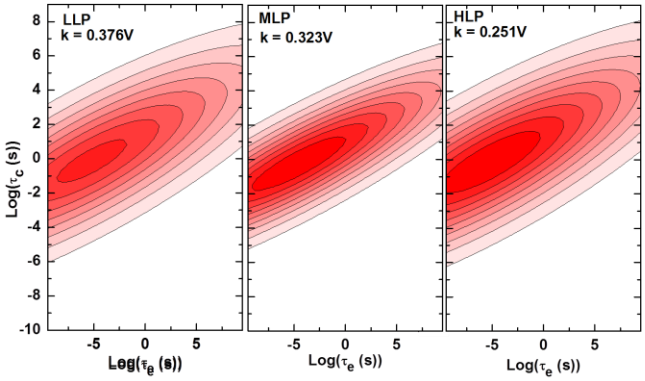

Fig. 4. Defect distribution in the τ_c-τ_e space. Similar distributions are obtained for the three laser powers considered. The k parameter (related to the number of defects in the device) decreases with the laser power.

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