ISDRS 2013, December 11-13. 2013

Built-In Self-Test Structure (BIST) for Resistive RAMs Characterization: Application to Bipolar OxRRAMs

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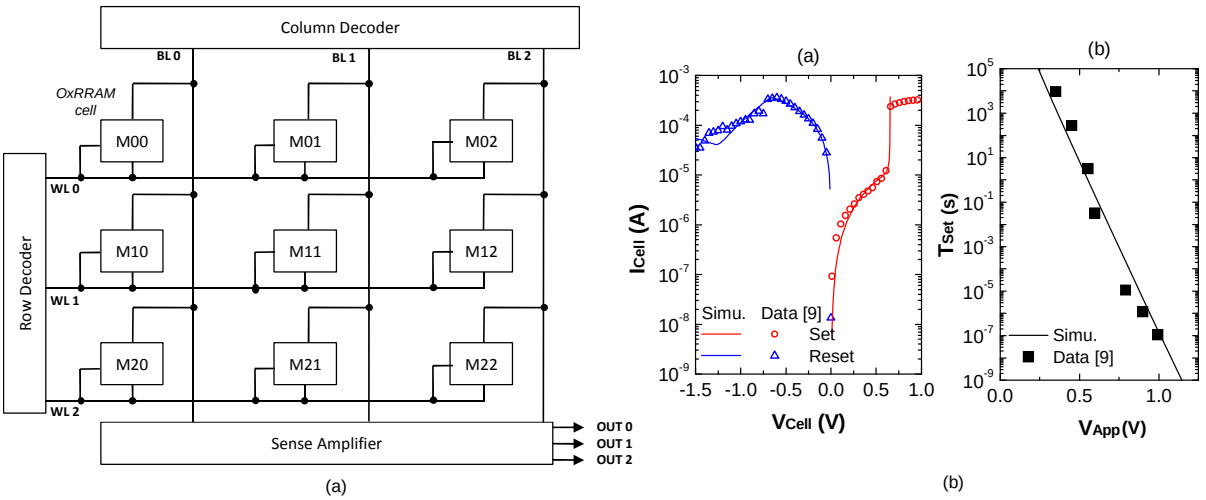
Problem Formulation: Resistive Random Access Memory (ReRAM) is a form of nonvolatile storage that operates by changing the resistance of a specially formulated solid dielectric material [1]. Among ReRAMs, Oxide-based Resistive RAMs (so-called OxRRAM) are promising candidates due their compatibility with CMOS processes and high ON/OFF resistance ratio. Common problems with OxRRAM are related to high variability in operating conditions and low yield. OxRRAM variability mainly impact ON/OFF resistance ratio. This ratio is a key parameter to determine the overall performance of an OxRRAM memory. In this context, the presented built-in structure allows collecting statistical data related to the OxRRAM memory array (ON/OFF resistance distributions) for reliability assessment of the technology.

Built-In Self-Test (BIST) structure: Fig. 1a presents the elementary array used for simulation which is constituted by a 3×3 1T/1R cell matrix, a row decoder, a column decoder and a sense amplifier for the read operation. The OxRRAM compact model used to build the memory array satisfactorily matches quasi-static and dynamic experimental data measured on actual HfO_2-based devices (Fig. 1b). Notice that the OxRRAM model allows a variability analysis based on OxRRAM card model parameters variation. The card model parameter variations are chosen to feet experimental data [2].
Fig. 2 presents the single-ended sense amplifier (solid line). The circuit working principle is quite simple. During a READ operation, the OxRRAM cell is biased throw the row decoder (with $V_{read} > 0$ and WL high). The current cell value I_{cell} is generated according to the memory state (RON≈7kΩ after a SET operation and ROFF≈25 kΩ after a RESET operation). The comparator input V_{IN} is directly proportional to I_{cell} and therefore to the OxRRAM resistance (two distinct values are available for V_{IN}: $V_{IN\ SET}$ for RON and $V_{IN\ RESET}$ for ROFF).
So that the sense amplifier operates properly, on the one hand the difference between $V_{IN\ SET}$ and $V_{IN\ RESET}$ must be the highest and on the other hand V_{REF} has to be set exactly between $V_{IN\ SET}$ and $V_{IN\ RESET}$ values.
At a circuit level, V_{IN} is the parameter to consider in terms of memory functionality. To extract V_{IN} value, a variable voltage reference source and a multiplexer are incorporated in the sensing circuit (dotted part of the circuit) and the READ operation is modified as follow:

- V_{REF} increases step by step from 0 to V_{dd} (V_{REF} increase is controlled by a shift register),
- V_{IN} value is detected when the sense amplifier output switches (the shifting process stops when $V_{REF} > V_{IN}$, *i.e* Rd_REG signal becomes active),
- V_{IN} is available at the circuit output in a numerical value when BIST_EN signal is high.

Simulation results:
To validate the BIST structure, a variability analysis is conducted through 500 Monte Carlo simulations. The elementary matrix presented in Fig. 1, embedding the BIST structure, is considered for simulations. As a result of cell variability, circuit performance exhibits much wider variability. In Fig. 3a, RON and ROFF distributions are plotted (RON/ROFF variability being correlated with actual silicon results). In Fig. 3b, $V_{IN\ SET}$ and $V_{IN\ RESET}$ distributions are also plotted. These last distributions are similar to RON and ROFF distributions. This trend is confirmed by the correlation curve presented in Fig. 4. Therefore, the modified sense amplifier structure can be used as a powerful tool to track any resistance variations but also to characterize the memory array variability.

To summarize, a built in self-test structure is presented for Resistive RAM characterization and variability evaluation. The area overhead introduced by structure is relatively low as the structure is integrated in the sense amplifiers. The normal mode of operation of the memory is preserved. Besides, extracted values are given in a digital data format, so the extraction process does not required any analog pin on the tester, making it fully digital tester compliant or easily observable via the random logic.



(a) (b)

Fig. 1 (a) OxRRAM memory array (a) I-V characteristic measured on HfO2-based devices and corresponding simulation using the OxRRAM model & SET voltage as a function of the programming ramp

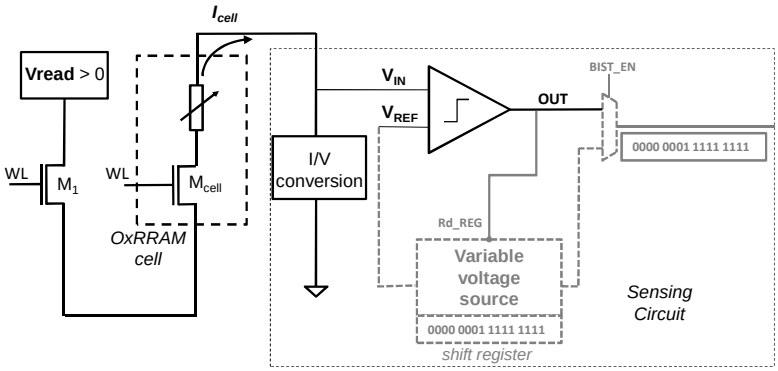


Fig. 2 Sense amplifier circuit

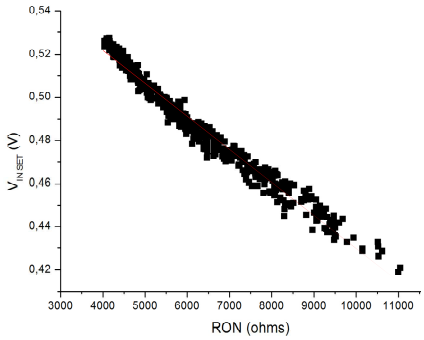


Fig. 4 RON versus $V_{IN\ SET}$ correlation graph

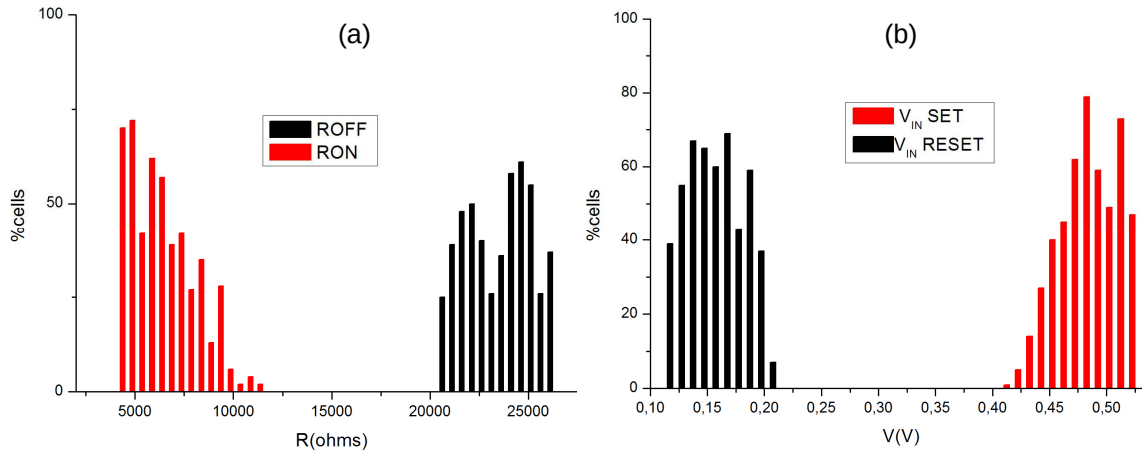


Fig. 3 RON and ROFF distributions & $V_{IN\ SET}$ and $V_{IN\ RESET}$ distributions versus cell variability

References

[1] J. F. Gibbons & al, “Switching properties of thin Nio films”, Solid-State Electronics, vol. 7, issue 11, pp. 785-790. (1964).

[2] H. Aziza & al, “Evaluation of OxRAM cell variability impact on memory performances through electrical simulations”, Non-Volatile Memory Technology Symposium. (2011).